

Application No.: 10/692,589

Docket No.: JCLA11007

**AMENDMENTS****In the Claims:****Claims 1-5 (canceled)**

Claim 6. (currently amended) A chip package structure,[[at least]] comprising:  
a hybrid integrated circuit (IC) carrier having a first surface and a second surface, wherein  
the hybrid IC carrier at least having:  
a plurality of patterned conductive layers stacked over each other, wherein the  
patterned conductive layer closest to the first surface furthermore has a plurality of  
bonding pads thereon;  
a plurality of dielectric layers respectively sandwiched between a pair of  
neighboring patterned conductive layers, wherein at least one of the dielectric layers is a  
ceramic dielectric layer with one ceramic dielectric layer positioned with all the  
remaining dielectric layers on one side thereof, and at least one of the remaining dielectric  
layers is an organic dielectric layer [[a plurality of dielectric layers respectively  
sandwiched between a pair of neighboring patterned conductive layer, wherein at least  
one of the dielectric layers is a ceramic dielectric layer with one ceramic dielectric layer  
as a dielectric core layer and at least one of the remaining dielectric layers is an organic  
dielectric layer, and wherein the dielectric layers are formed via a built up method]]; and

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a plurality of vias passing through at least the dielectric core layer for connecting at least two of the patterned conductive layers electrically; and a chip attached to the first surface of the hybrid IC carrier and connected electrically to the hybrid IC carrier via the bonding pads, wherein the ceramic dielectric layer is attached to the chip on the first surface of the hybrid IC carrier.

**Claims 7-10. (canceled)**

Claim 11. (original) The chip package structure of claim 6, wherein the chip is electrically connected to the hybrid IC carrier through a flip chip bonding or a wire bonding process.

Claim 12. (original) The chip package structure of claim 6, wherein the package furthermore comprises a plurality of contacts attached to the second surface of the hybrid IC carrier.

**Claim 13. (canceled)**